REMARKS

The present Amendment is submitted under the provisions of 37 CFR 1.312(a). It is requested that the present Amendment be entered since the present Amendment will not require any substantial amount of additional work on the part of the Examiner.

The above amendments to the specification are presented in order to make minor editorial revisions. The changes made are non-substantive in nature and do not add new matter. Enclosed is a marked-up copy of sections of the original specification and claims 2 and 5-7, labeled "**Version with Markings to Show Changes Made**" indicating the same changes. The amendments to claims 2 and 5-7 do not alter the scope of the claims, and therefore will not require any additional search or examination by the Examiner. Since the scope of the claims has not been changed, the claims remain patentable for the original reasons for allowance. The present Amendment was not submitted earlier since the necessity of the amendments was not earlier noticed and the application was allowed in the first Office Action on the merits.

Therefore, it is respectfully requested that the present Amendment be entered as being directed to matters of form not affecting the scope of the invention.

Respectfully submitted,

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extracts the DC component of the output signal from A/D converter 8. D/A converter 10 converts the digital output signal from offset control circuit 9 to an analog voltage. Signal processor 11 processes the output signal from A/D converter 8. PLL circuit 12 applies frequency control based on the output signal from the wobble digitizer 19, further described below, applies phase control using the output signal from A/D converter 8, and generates a clock synchronized to the A/D converter signal.

(8) As shown in Fig. 1, differential amplifier 7, A/D converter 8, offset control circuit 9, and D/A converter 10 form an "offset control loop." Providing an offset control loop makes it possible to control the center of DC level fluctuation in the signal input to A/D converter 8 to approximately the center of the range of voltage levels (hereinafter referred to as "conversion level") that can be converted by A/D converter 8. The value of the conversion level center point output by A/D converter 8 after analog-to-digital conversion has a value of 0, where voltage values below this center point are output as negative values, and voltage values above this center point are output as positive values.

A process whereby preamplifier 3 of signal output unit 30 outputs the TE signal and RF signal is described below. Preamplifier 3 contains a focus detector (not shown in the figure) having four sensors (sensors A, B, C, D). The signal read beam emitted from the optical pickup 2 is reflected from optical disc 1 and incident to the focus detector. The focus detector detects the signal read beam using the four sensors A to D. An RF signal can therefore be obtained by adding all outputs from focus detector sensors A to D.

(24) The section shape of the reflected light is a regular circle when the light beam is focused on a pit, and is elliptical when not focused on a pit. Each

of the four focus detector sensors output the same detection signal when the reflected beam is circular, and output different detection signals when the reflected beam is elliptical. Assuming that sensors A and B detect the reflected light lopsided toward the inside circumference of the track and sensors C and D detect the reflected light lopsided toward the outside circumference of the track. The output signal of sensor A is denoted as "A", and the like, and a TE signal can obtained by (A+B)-(C+D).

The format of an optical disc 1 to which the data that is reproduced by optical disc apparatus 100 according to this preferred embodiment of the invention is described next below. Fig. 2 is a schematic diagram showing the data format of a circular optical disc 1 such as a DVD-RAM disc. Optical disc 1 is broadly divided between a header area 81 for storing address information, and a content storage area 82 to which is recorded the video, audio, and other content that a user will want to reproduce.

Grooves 33 and lands 34 are alternately disposed in the content storage area 82. Address information in header area 81 is divided into streams IDa and IDb, which are disposed with one offset 1/2 track pitch to the inside or outside circumference side of the other. The pit signal width in this header area 81 is controlled to substantially the same width as the grooves 33 and lands 34 in the content storage area 82.

It will be noted that while plural sectors appear to be present only in content storage area 82, each defined sector includes a header area 81 part and a content storage area 82 part. That is, header area 81 is part of a sector.

As will be known from Fig. 2, grooves 33 and lands 34 wobble in a sine wave pattern orthogonally to the track trace. An advantage of this is that

recording time can be shortened by detecting the period of this sine wave wobble signal, generating a clock synchronized to the detection signal, and writing data synchronized to this clock. This is because wobble appears substantially continuously in one rotation of grooves 33 and lands 34, and wobble PLL circuit for generating recording clocks (not shown) can therefore quickly lock onto the phase.

The operation of a optical disc apparatus 100 (Fig. 1) for reproducing content from optical disc 1 is described next below with reference to Fig. 3.

Fig. 3 is a timing chart used to describe the operation of optical disc apparatus 100 (Fig. 1), and the corresponding sector format. The following example further assumes that data is read from a DVD-RAM disc. Row (g) in Fig. 3 corresponds to the data structure in Fig. 2. The prepits formed in header area 81 are broadly grouped as VFO parts 83a, 84a, 85a, and 86a recording a single frequency pattern, and address ID parts 83b, 84b, 85b, and 86b recording address information.

Content storage area 82 is readable and writable, and data may or may not be recorded to content storage area 82. When data is recorded, content storage area 82 contains a first guard area 87, VFO 88, the recorded content (user data) 89, and second guard area 90. Content storage area 82 has a periodically wobbling format with the wobble period being the 186 channel clock period as shown in Fig. 3. Therefore, regardless of whether data is recorded to the content storage area 82, the TE signal contains both the prepit signal corresponding to the header area 81 as shown in (b) in Fig. 3, and a wobbling sine wave signal having a period of 186 channel clocks.

As shown in (h) in Fig. 3, header area 81, identified by IDa in Fig. 2, contains VFO 83a, address ID 83b, VFO 84a, and address ID 84b. Header area 81 likewise contains VFO 85a, address ID 85b, VFO 86a, and address ID 86b.

A normal reproduction operation is described first below with reference to Fig. 1.

The read signal from optical disc 1 generated by optical pickup 2 is input to preamplifier 3. Preamplifier 3 outputs an RF signal ((a) in Fig. 3) and TE signal ((b) in Fig. 3). As shown in the figure, these signals have a high level (= 1) signal level when header area 81 is read. This is because header area 81 is manufactured with high reflectivity. The RF signal is input to clamping unit 4 and amplitude fluctuation detector 14. The TE signal is input to clamping unit 4, wobble dropout detector 16, and wobble digitizer 19.

The RF signal, TE signal, header gate signal ((d) in Fig. 3), read gate signal ((e) in Fig. 3), and selector 18 output signal are input to clamping unit 4. Fig. 4 is a circuit diagram showing the configuration of clamping unit 4. Clamping unit 4 contains selector 21, capacitor 22, resistors Ra 23 and Rb 24, clamping switch 25, OR gate 26, inverter 27, and buffer 28. Selector 21 time division switches between the RF signal and TE signal based on the header gate signal from controller 13 (Fig. 1). Capacitor 22 cuts the DC component of the output signal from selector 21. Resistors Ra 23 and Rb 24 apply a desired DC potential to the output signal from capacitor 22. Note that Rb is sufficiently low compared to Ra. For example, Rb ≈ Ra/10. Capacitor 22 and resistor Ra 23 or resistor Rb 24 form a bypass filter.

Clamping switch 25 closes when a high level (= 1) input signal is

applied. Resistor Rb shorts to a specific potential Vcen when clamping switch 25 closes. This time-division reduces the time constant determined by capacitor 22 and resistor Ra 23 or resistor Rb 24, enabling DC fluctuation to be quickly suppressed. OR gate 26 and inverter 27 are a logic circuit for aligning the polarity of and merging the output signal from selector 18 (Fig. 1) and the control signal from controller 13 (Fig. 1). More specifically, OR gate 26 outputs a 1 when the output signal from selector 18 (Fig. 1) is 1 or the read gate signal is 0. Buffer 28 buffers the clamped signal.

The operation of a clamping unit 4 thus comprised is described next below. Selector 21 selects the TE signal when the header gate signal ((d) in Fig. 3) is high level (= 1), and selects the RF signal when the header gate signal is low level (= 0). The header gate signal goes high level (= 1) when optical disc apparatus 100 (Fig. 1) reproduces the header area 81 of the disc.

It is important to note here that when the header gate signal is high level (= 1), there is no sharp DC fluctuation in the output signal from clamping unit 4 ((c) in Fig. 3) even if there is sharp DC fluctuation in the TE signal ((b) in Fig. 3). This is because DC fluctuation causes the read gate signal ((e) in Fig. 3) to go low level (= 0) and clamping switch 25 therefore closes. More specifically, as a result of clamping switch 25 closing and resistance Rb 24 shorting to voltage Vcen, the time constant determined by the sufficiently low resistance Rb 24 and capacitor 22 is small, and DC fluctuation is quickly suppressed.

(83) The read gate signal ((e) in Fig. 3) goes between the high level and low level three times in one sector. That is, the read gate signal rises slightly delayed from the start of VFO 83a and 85a, falls at the end of address information 84b

and 86b, rises slightly delayed from the beginning of VFO 88, and falls in second guard area 90. Note that approximately the center of the amplitude variation of output signal from clamping unit 4 shown in (c) in Fig. 3 is matched to voltage Vcen.

Referring again to Fig. 1, wobble digitizer 19 outputs a binary wobble signal ((f) in Fig. 3) to PLL circuit 12. PLL circuit 12 controls frequency by counting and comparing the period of this binary wobble signal with its own clock. As shown in Fig. 1, PLL circuit 12 also receives the read gate signal from controller 13 and performs feedback control so as to synchronize with a predetermined reference phase. When the feedback signal synchronizes with the reference phase, PLL circuit 12 locks the phase of the feedback signal. An RF signal output from A/D converter 8 and sampled at the output clock of PLL circuit 12 is input to PLL circuit 12. When the frequency enters the capture range as a result of the above-noted frequency control, PLL circuit 12 applies phase control and sets the zero cross point sample value to zero. PLL circuit 12 also generates and supplies to other components a clock synchronized to the RF signal. Signal processor 11 applies Viterbi decoding, demodulation, or other process, and outputs address information and user data to controller 13 and other downstream circuits (not shown in the figure).

A method whereby A/D converter 8 cancels input signal offset is described next. A/D converter 8 outputs an A/D converted signal to offset control circuit 9. Offset control circuit 9 counts each sign change in the polarity signal (MSB) of this digital signal at the channel clock. More specifically, offset control circuit 9 increments the count at each positive sign and decrements the count at each negative sign. The offset control circuit 9 repeats these addition

fluctuation detector 14 (Fig. 1), first detection signal delay 15 (Fig. 1), wobble dropout detector 16 (Fig. 1), and second detection signal delay 17 (Fig. 1) detect DC level fluctuation in the playback signal from the optical disc, and generate a detection signal that tracks this fluctuation.

When the sector containing period D where the black dot is present is read, light is not reflected only where the black dot is present, and the RF signal level thus swings to the low side (dark reflection) ((j) in Fig. 5). The TE signal also drops where the black dot is present ((p) in Fig. 5). Clamping unit 4 is a high pass filter with a large time constant relative to the sector length in the steady state, and the output signal at this time is a differentiated signal as shown in (k) in Fig. 5.

(12) Amplitude fluctuation detector 14 detects the upper envelope, which is the output when the RF signal reflection is bright, and slices the envelope signal at a fixed level. Parts lower than the slice level are output as a "1", and higher parts are output as a "0" ((m) in Fig. 5). This means that output goes high level (= 1) when the black dot is read, and then goes low level (= 0) after the black dot is passed. Wobble dropout detector 16 full-wave rectifies the TE signal. That is, wobble dropout detector 16 inverts signals below a specific reference level to a signal level above this reference level to generate a full-wave rectified signal. Wobble dropout detector 16 slices this full-wave rectified signal at a fixed level, and outputs parts below the slice level high level (= 1) and parts above the slice level low level (= 0) ((q) in Fig. 5). As with output from amplitude fluctuation detector 14, output goes to the high level (= 1) when the black dot is read, and then goes to the low level (= 0) after passing the black dot.

First detection signal delay 15 extends the high level (= 1) period

When a read error occurs, controller 13 (Fig. 1) controls selecting a total of five signal types, that is four types of signals and a null signal, sequentially or according to whether reproduction is possible. Control is based on control signals generated by controller 13. This makes it possible to improve the read performance of optical disc apparatus 100 (Fig. 1).

First, data is read from optical disc 1 (Fig. 1) to generate an RF signal (step S602). This RF signal is shown in (j) in Fig. 5. When the RF signal is obtained, controller 13 (Fig. 1) instructs selector 18 (Fig. 1) to select a low level signal and determines whether reproduction (reading) is possible using that RF signal (step S604). This low level signal is a null signal without valid polarity, and means that clamping is not applied. Null signal selection is possible because there are cases, such as when fine amplitude variation continues for an extended time due to, such as, fingerprints, when reading is easier if clamping is not applied even though amplitude variation is detected. If the null signal is selected, the waveform of the output signal from clamping unit 4 (Fig. 1) is as shown in (k) in Fig. 5. When a signal such as this is output from clamping unit 4 (Fig. 1) and as a result, reproduction is possible, control skips to the subsequent signal processing operation (step S616) of the signal processor 11 (Fig. 1).

However, as previously described with reference to (t) in Fig. 5, if the output signal from clamping unit 4 is input to A/D converter 8 and this input signal exceeds the reference level of A/D converter 8, that part of the signal above the reference level cannot be reproduced. In this case, the same selection signal (that is, a null signal) is output again (step S606). This is because the first reproduction attempt may simply fail accidentally.

to reproduce media, such as DVD-RAM discs, containing a wobble signal. Amplitude fluctuation detector 14 is, however, required to play media not containing a wobble signal, such as DVD-ROM discs.

It will also be noted that while an offset loop is used in this preferred embodiment of the invention, an offset loop is not necessarily required.

EMBODIMENT 2

Fig. 7 is a block diagram showing the playback mechanism of an optical disc apparatus 700 according to a second embodiment of this invention. Like parts in this and the first embodiment shown in Fig. 1 are identified by like reference numeral, and further description thereof is omitted below.

Optical disc apparatus 700 according to this second embodiment differs from the optical disc apparatus 100 (Fig. 1) of the first embodiment in that (1) clamping unit 4 (Fig. 1) comprises only selector 21; (2) amplitude fluctuation detector 14, first detection signal delay 15, wobble dropout detector 16, second detection signal delay 17, and selector 18 are eliminated; and (3) comparator 41, digital voltage generator 42, and second differential amplifier 43 are disposed between equalizer 6 and differential amplifier 7.

(19)

The functions of the new elements noted in (3) above are described below. Output signal from equalizer 6 and the digital voltage signal from digital voltage generator 42 are input to comparator 41 and second differential amplifier 43. Comparator 41 compares the output signal from equalizer 6 and the output signal from digital voltage generator 42. If the output signal from equalizer 6 is greater, comparator output signal s goes to the high level (= 1), and otherwise goes to the low level (= 0). Comparator 41 also outputs the

inversion t of output signal s. Both output signals s and t are input to digital voltage generator 42. Digital voltage generator 42 is provided to maintain the duty ratio between 1s and 0s in the comparator 41 output signals to a specific value (such as 1 in this example) based on the read gate signal from controller 13. More specifically, digital voltage generator 42 outputs the difference between output signal s and inverse signal t from comparator 41. The output signal from digital voltage generator 42 is input to second differential amplifier 43 and as feedback to the comparator 41. Second differential amplifier 43 outputs the difference of the digital voltage output signal from digital voltage generator 42 subtracted from the output signal from equalizer 6.

Fig. 8 shows the configuration of digital voltage generator 42 in detail. Digital voltage generator 42 has a differential amplifier 421, analog switch 422, resistor Rc 423, resistor Rd 424, inverting integrator 425, and inverting amplifier 426. Differential amplifier 421 compares output signals s and t from comparator 41 (Fig. 7), outputs high level (= 1) if output signal s is higher, and outputs low level (= 0) if output signal s is lower. Analog switch 422 switches the circuit according to whether the read gate signal is 0 or 1. That is, analog switch 422 closes to resistor Rc 423 when the read gate signal is high level (= 1), and closes to resistor Rd 424 when the read gate signal is low level (= 0). Note that Rd is here sufficiently low compared with Rc. For example, preferably Rd $\approx$ Rc/10. This ensures rapid signal tracking when the read gate signal is low level (= 0) because the signal passes the sufficiently low resistor Rd 424. Signals passing resistor Rc 423 or resistor Rd 424 are sequentially input to the series connected inverting integrator 425 and inverting amplifier 426. Inverting integrator 425 and inverting amplifier 426 charge the high level

difference between output signals s and t from comparator 41 (Fig. 7) and a specific reference level to the capacitor of inverting integrator 425, and also output the difference.

Operation of optical disc apparatus 700 (Fig. 7) is described next with reference to Fig. 9. Fig. 9 is a timing chart used to describe the operation of optical disc apparatus 700 (Fig. 7). The differences between Fig. 9 and Fig. 3 are due to the above-noted differences (2) and (3) between optical disc apparatus 100 (Fig. 1) and optical disc apparatus 700 (Fig. 7). Fig. 9 additionally shows the waveforms of the output signal ((v) in Fig. 9) from selector 21 (Fig. 7), the output signal ((w) in Fig. 9) from digital voltage generator 42 (Fig. 7), the output signal ((s) in Fig. 9) from comparator 41 (Fig. 7), and the output signal ((x) in Fig. 9) from second differential amplifier 43.

A normal playback operation is described first with reference to Fig. 7. The optical disc 1 read signal captured by optical pickup 2 is first input to preamplifier 3. Preamplifier 3 outputs an RF signal ((a) in Fig. 9) and TE signal ((b) in Fig. 9). Controller 13 applies the header gate signal ((d) in Fig. 9), which goes high level (= 1) only in the header area 81 (Fig. 3), to selector 21. Selector 21 selects the TE signal only while the header gate signal is high level (= 1), and selects the RF signal when the header gate signal goes low level (= 0).

The read gate signal ((e) in Fig. 9) is input to digital voltage generator 42. The read gate signal shown in (e) in Fig. 9 is effectively the same as the read gate signal shown in (e) in Fig. 3 and described in the first embodiment above. That is, this read gate signal ((e) in Fig. 9) rises and falls three times in one sector. In other words, the read gate signal rises slightly delayed from the start of VFO 83a and VFO 85a, falls at the end of address